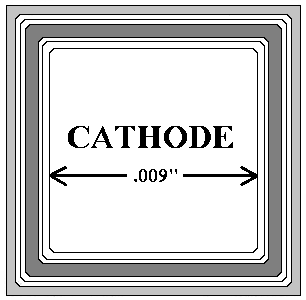
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.015”**



**.015”**

**\*\*REVERSED ANODE ON BACKSIDE\*\***

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .009” X .009”**

**Backside Potential: Anode**

**Mask Ref: TTU**

**APPROVED BY: DK DIE SIZE .015” X .015” DATE: 12/19/22**

**MFG: SPRAGUE / ALLEGRO THICKNESS .007” P/N: 1N914-R**

**DG 10.1.2**

#### Rev B, 7/19/02